UNIVERSITY OF ESWATINI
FACULTY OF SCIENCE AND ENGINEERING
DEPARTMENT OF PHYSICS

MAIN EXAMINATION, DECEMBER 2018

TITLE OF PAPER	:	DIGITAL ELECTRONICS 1
COURSE NUMBER	:	PHY 411
TIME ALLOWED	:	THREE HOURS
INSTRUCTIONS	:	Answer **FOUR** (4) questions only.
	:	Each Question carries **25 Marks**
	:	Marks for different Sections are shown in far Right margin.

THIS PAPER HAS 5 PAGES, INCLUDING THIS ONE.

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1. (a) Convert the hexadecimal number $2B6D.5AB_{16}$ to its equivalent decimal number. [3]

   (b)Subtract $(-14)_{10}$ from $(-24)_{10}$, using the 2's complement representation. [6]

   (c) State De Morgan's theorems. [2]

   (c) Simplify the following expressions using Boolean algebra:

   (i) $F = (X + \overline{Y} + \overline{X}.Y).\overline{Z}$ [5]

   (ii) $F = \overline{X}.Y(X + \overline{Y} + \overline{X}.Y).(X + \overline{Y})$ [3]

   (d) Indicate how a NAND gate can be used to implement:

   (i) An Inverter. [2]

   (ii) An AND gate. [2]

   (iii) An OR gate. [2]

2. (a) Explain what is meant by the following terms;

   (i)Prime Implicant. [1]

   (ii) Essential Prime Implicant. [1]

   (iii) Distinguished 1-Cell. [1]

   (b) Consider the logic function Y described by the truth table below.

Y	0	1	0	1	1	0	1	1	0	1	1	1	1	1	0	0
D	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
C	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
B	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

   (i) Write this function in disjunctive normal form (DNF). [4]

   (ii) Simplify this expression by using a Karnaugh map. [8]

   (c) Give the maxterm Boolean function expressed by [4]

$$F(A, B, C) = \prod M(O, 3, 7)$$

   (d) Using the Karnaugh Map, find a minimum sum-of-products expression for the following logic function [6]

$$F(W, X, Y, Z) = \sum m(0, 1, 3, 5, 14) + d(8, 15)$$

3. (a) Show two possible arrangements of the hardware-implementing of a four-input OR gate, using two-input OR gates only. [4]

   (b) The truth table below gives the output F, for inputs A and B. What logic gate would perform this operation? Draw a symbol for this gate. [3]

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

(c) Apply suitable Boolean laws and theorems to modify the expression for a two-input EX-OR gate, $F = A \bigoplus B = A\overline{B} + B\overline{A}$ in such a way as to implement a two-input EX-OR gate by using the minimum number of two-input NAND gates only. [7]

(d) Use maxterms (not minterms) and a Karnaugh map to convert the Boolean expression,

$$y = C + A\overline{B} + B\overline{A}$$

into a canonical POS form. [7]

(e) Write the simplified Boolean expression $F(A, B, C, D)$ for the Karnaugh map shown in Figure 1. [4]

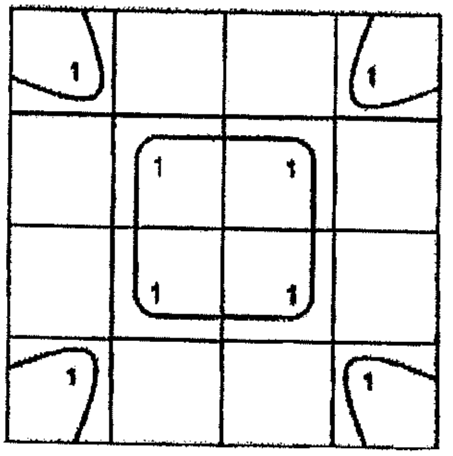


Figure 1:

4. (a) Explain what is meant by 'level triggering','negative-edged triggering' and leading-edge triggering of a flip-flop. [6]

(b) Figure 2 is a logic diagram of a D-type flip-flop. Answer the following questions with reference to the figure;

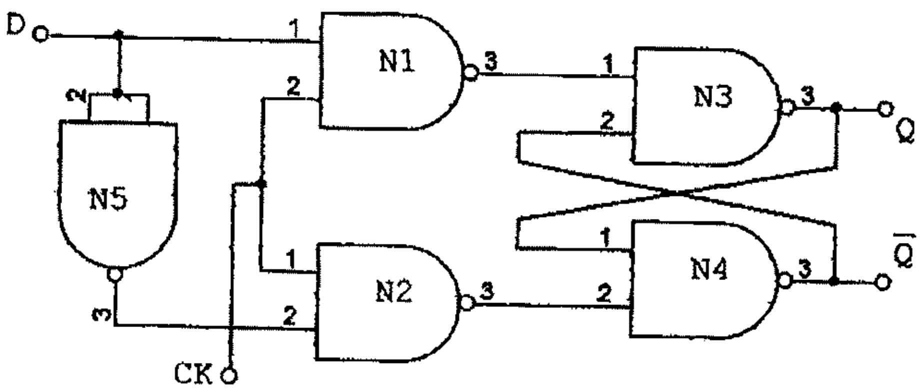


Figure 2:

(i) What is the advantage of having a single input to the latch? [2]

(ii) What is the function of the gate labeled N5? [1]

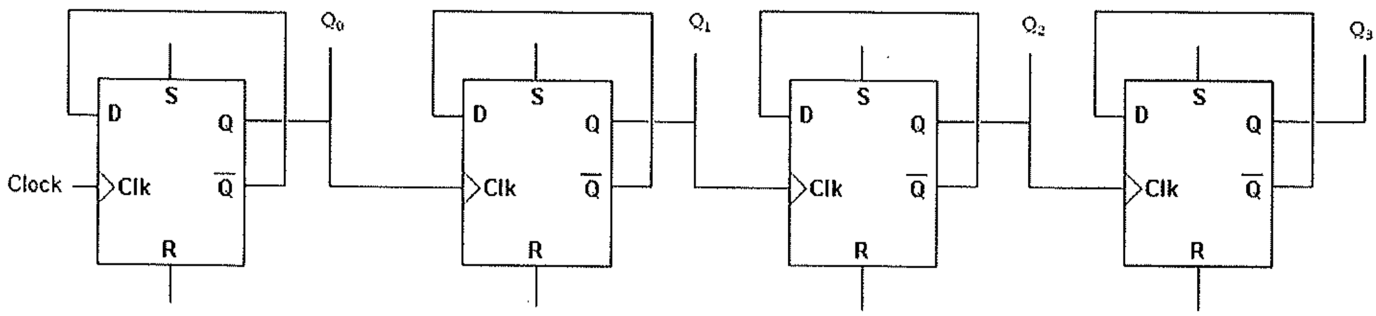
(iii) Complete the table in Figure 3 for the various signals applied to the inputs. [4]

Figure 3:

Input			Outputs before the clock pulsed		Outputs after the clock pulsed	
D	S	R	Q	Q'	Q	Q'
0	0	1	1	0		
0	0	1	0	1		
1	1	0	1	0		
1	1	0	0	1		

(c) Consider the D-flip-flops in the Figure 4 below and assume that the initial state of Q0, Q1, Q2, and Q3 are all logical zeros.

Figure 4:



(i) Draw the timing diagram for the counter, indicating the clock and the outputs. [5]

(ii) After how many clock pulses will Q3 change state from 1 to 0? [2]

(d)

(i) Differentiate between the truth table and the excitation table. [3]

(ii) Draw a well labeled excitation table for a D-Flipflop. [2]

5. (a) Differentiate between Synchronous and Asynchronous Counters. [2]

(b) Determine the number of flip-flops required to construct a MOD-10:

(i) Ring counter; [5]

(ii) Johnson counter. [5]

Also write the count sequences in the two cases .

(b) Give two uses of shift registers. [2]

(c) Describe the functions of the following elements of a microprocessor unit:

(i) Data register (DR); [1]

(ii) Address register (AR); [1]

(iii) Arithmetic logic unit (ALU); [1]

(iv) Stack Pointer (SP). [3]

(e) Name five flag registers of the microprocessor and state how they work. [5]

END