UNIVERSITY OF SWAZILAND

FACULTY OF SCIENCE
Department of Electrical and Electronic Engineering

July 2014
SUPPLEMENTARY EXAMINATION

Title of the Paper: **DIGITAL SYSTEMS II**
Course Number: **EE324**
Time Allowed: **Three Hours.**

Instructions:
1. To answer, pick any to sum a total of 100% from
7 questions in the following pages.
If answer more than 100%, cancel by the grade marker the question of the best score answered. Never try to risk and take chances.
2. The answer is better neatly written in the space provided in the question book. Use the answer book as a scratch pad.
3. This paper has 8 pages, including this page.

DO NOT OPEN THE PAPER
UNTIL PERMISSION HAS BEEN GIVEN BY THE INVIGILATOR.

Q1. (a)10%: Draw a block to show all control signal, data input and data output for a universal register.

(b)10%: Using the above register to implement the hardware of the following statement. Include the logic gates for the control function. In the statement, the D is a D/ff and AR a 4-bit register.

Statement: if (D=0) then ($AR \leftarrow C_{hex}$) else ($AR \leftarrow 0_{hex}$).

Q2. Transfer this state table on the right into **(a)10%:** state diagram and **(b)10%:** state equations.

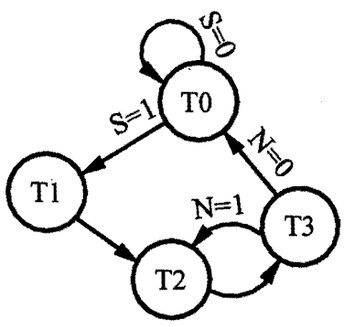
PS,	in	NS	ot
001,	0	001	1
001,	1	010	1
010,	0	011	0
010,	1	110	0
011,	0	001	0
011,	1	100	0
100,	0	110	0
100,	1	100	1
110,	0	001	0
110,	1	100	1

Q3. 20%: Implement a circuit to generate and display a sequence F0C4, F0C4, ---. Treat the not-used states to make the sequencer a self-starting machine. You are free to choose the type of ff to use. (hint: you may consider F0C4 as 4 codes and use two ff's to code the 4 codes; then there is no not-used states and hence a self-starting machine. Finally, convert the 4 codes into F0C4 to display.)

Q4. Shown on the right is a 4-state state diagram of a control unit where control inputs are S, N, and Q_1 and output is $L=Q_1T_2$. Design the control circuit by the sequence register and decoder structure with two JK ffs G_2 and G_1.

(a) 10%: Use the decoder outputs as conditions for the present states.

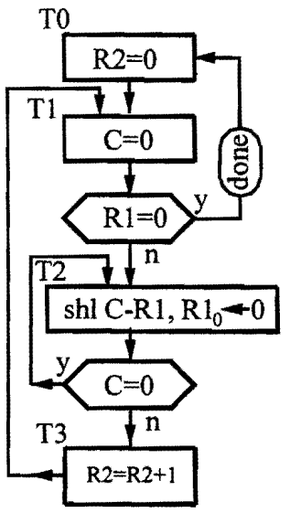
(b) 10%: Use the ff outputs as conditions for the present states.



Q5. Shown on the right is the flowchart of a digital system that counts the 1's in the Register R1 and the total count is stored in R2. Appended on the left to R1 is a one bit carry register C.

(a)10%: List the register transfer statements to be executed in each control state,

(b)10%: Draw a state diagram for the controll.



Q6. 20%: There are 8 1-digit BCD numbers in random order to be arranged into the sequence of descending magnitude order. Consider the 4-bit magnitude comparator as one block. Design the ASM chart to do the work.

Q7. 20%: A bit-serial byte adder of the block diagram in Fig. 7 receives two external input bits x and y; the third input C_i comes from the output of a D/ff. The carry output is transferred to the ff every clock pulse. The external S output gives the sum of x, y, and C_i. Obtain the state table and state diagram of the sequential circuit.

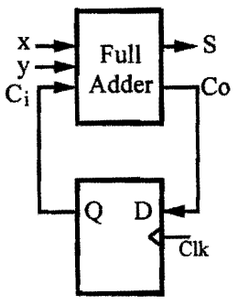


Fig. 7