UNIVERSITY OF ESWATINI

Faculty of Science and Engineering Department of Computer Science

MAIN EXAMINATION

DECEMBER 2019

Title of Paper: COMPUTER ORGANIZATION AND ARCHITECTURE II

Course Code: CSC 321

Time Allowed: 3 Hours

Total Marks: 100

Instructions to Candidates:

This Question Paper Consists of FIVE (5) Questions. Section A is compulsory.

Answer ALL Questions in SECTION A and ONE Question from SECTION B.

Marks are indicated in Square Brackets.

NB: You Are Not Allowed To Open This Examination Paper Until Permission Has Been Granted By The Invigilator

SECTION A

Qu€	uestion One [30]				
1.	Define the following terms: a. Data path [1] b. Assembly language [1] c. Microarchitecture level [1]				
2.	State the three (3) elements have to be considered when designing the microarchitecture level. [3]				
3.	State any four (4) advantages of compilers. [2]				
4.	4. Describe any two (2) factors that makes a good ISA. [2]				
5.	5. Briefly explain why it is not a good idea to have the hardware directly execute high level languages. [2]				
6.	Is it possible to have zero-address instruction? Explain your answer.	[3]			
7.	Explain the purpose of the following instructions: a. Arithmetic instructions [1] b. Logic instructions [1] c. Test Instructions [1] d. Memory instructions [1] e. I/O instructions [1] f. Branch Instructions [1]				
8.	List the three (3) main things that are compiler writer should know.	[3]			
9.	Briefly describe any two (2) addressing modes. [6]				
ues	stion Two	[30]			
1.	Briefly describe how the two-pass assembler works. [3]				
2.	Write the assembly language equivalent of the following instructions: a. 001000000000111 [2] b. 1001000000001011 [2]				
3.	Draw the instruction state diagram. [4]				
4.	List the four (4) categories of microoperations. [4]				

- 5. State and describe the two (2) basic tasks that can be performed by a control unit. [4]
- 6. Write a MARIE program using a loop that multiplies two positive numbers by using repeated addition. For example, to multiply 3 × 6, the program would add 3 six times: 3+3+3+3+3. [5]
- 7. Show the Register Transfer Notation (RTN) including the contents of registers for the following program. [6]

Label	Hex Address	Instruction
	100	Load A
	101	Add One
	102	Jump S1
S2	103	Add One
	104	Store A
	105	Halt
S1,	106	Add A
	107	Jump S2
Α,	108	HEX 0023
One,	109	HEX 0001

Question Three

[15]

- 1. Define the following terms:
 - a. Multicore
- [1]
- b. Simultaneous multithreading [1]
- 2. Briefly describe any two (2) applications that benefit directly from the ability of scale throughput with the increase in number of cores. [2]
- 3. Describe any three (3) advantages of the use of higher-level cache on the chip. [3]
- 4. List the four (4) general organizations for multicore systems.
 - [4]
- 5. List key features of the Heterogeneous System Architecture (HSA).
- [4]

SECTION B

Que	stion Four	[25]
1.	Define the following terms: a. Interactive system [1] b. Uniprogramming [1]	
2.	Briefly explain any three (3) services provided by the operating system.	[3]
3.	List three (3) interfaces found on a typical computer system. [3]	
4.	Describe the two (2) main problems found in early computer system.	[4]
5.	Briefly describe the purpose of the following features in a batch system: a. Memory protection [2] b. Privileged instructions [2]	
6.	Briefly describe long-term scheduling. [4]	
7.	State three reasons that causes the execution of a process to be suspended	. [3]
8.	Briefly describe any two (2) advantages of segmentation to the programm	er. [2]
8.	Briefly describe any two (2) advantages of segmentation to the programm	er. [2]
	Briefly describe any two (2) advantages of segmentation to the programm	er. [2]
Ques	Define the following terms: a. Process [1] b. Thread switch [1] c. Uniform Memory Access	
Ques	Define the following terms: a. Process [1] b. Thread switch [1] c. Uniform Memory Access d. Nonuniform Memory Access	[25]
Que : 1.	Define the following terms: a. Process [1] b. Thread switch [1] c. Uniform Memory Access d. Nonuniform Memory Access Describe any four (4) methods of parallel processing. [4]	[25]
2. 3.	Define the following terms: a. Process [1] b. Thread switch [1] c. Uniform Memory Access d. Nonuniform Memory Access Describe any four (4) methods of parallel processing. [4] Briefly describe the key design issues of a multiprocessor operating system	[25]

MARIE INSTRUCTION SET

Mnemonic	Binary	Hex	Explanation
JnS	0000	0	Store the PC at address X and jump to X+1
Load X	0001	1	Load the contents of address X into A
Store X	0010	2	Store the contents of AC at address X
Add X		3	Add the contents of X to AC and store the result in AC
Subt X	0100	4	Subtract the contents of address X from AC and store the result in AC.
Input	0101	5	Input a value from the keyboard into AC
Output	0110	6	Output the value in AC to the display.
Halt	0111	7	Terminate the program.
Skipcond	1000	8	Skip the next instruction on condition
X qmuU	1001	9	Load the value of X into PC.
Clear	1010	Α	Put all zeros in AC
AddI X	1011	В	Add indirect: Use the value at X as the actual address of the data operand to add to AC
JumpI X	1100	С	Use the value at X as the address to jump to
LoadI X	1101	D	Load indirect: Use the value at X as the address of the value to load.
StoreI X	1110	E	Store indirect: Use X the value at X as the address of where to store the value