University of Swaziland

Department of Computer Science

Final Examination

December 2011

TITLE OF PAPER:	COMPUTER ORGANISATION II
COURSE NUMBER:	CS 341
TIME ALLOWED:	3 HOURS
INSTRUCTIONS:	ANSWER **SECTION A, AND,** ANSWER **THREE** QUESTIONS FROM **SECTION B**

This examination paper should not be opened until the invigilator grants permission.

SECTION A

Question 1 (COMPULSORY)

A) An instruction set has 4 bits for *opcode* and 32 bits for addresses. What percentage change in instructions and memory resolution results if the *opcode* is increased by 2 bits without altering the instruction length (by taking bits from address portion). [4]

B) Compare using the aid of suitable diagrams:

i). multiprocessor and multicomputer [4]
ii). Strict consistency and release consistency [4]
iii). Direct addressing and register indirect addressing [4]
iv). Cache miss and page fault [4]
v). Conditional and unconditional branching [4]

C) Convert the infix formula (a+cd)/x to postfix [1]

SECTION B (ANSWER ANY THREE QUESTIONS FROM THIS SECTION)

Question 2

A) Describe the 3 differences between **programmed I/O** and **DMA I/O** [6]

B) Describe, with the aid of diagrams, the following allocation algorithms:

i. First fit
ii. Best fit
iii. Worst fit [12]

C) Assume you have an expanding *opcode* that supports the following formats, with a 3 bit register:

4 instructions with 3 registers
255 instructions with one register
16 instructions with zero registers

i. How many *opcodes*, in total, does the preceding require? [3]
ii. How many **bits** does the *opcode* require to support the 3 formats? [3]

D) Why does the Intel have segment registers and the SPARC not? [1]

Question 3

Describe in less than 50 words each, using correct terminology and illustrations:

A) Segmentation. [10]
B) Paging. [10]
C) Paged segmentation. [5]

Question 4

a) A program takes 10 months to write in a high level language and takes 200 seconds to complete it's task. Two modules are responsible for 40% and 20% of the execution time of the program, respectively. These modules are of roughly equal complexity and account for 20% (each) of the total development effort. The compiler used can produce symbolic assembly language, so it only takes twice as long to tune the assembly language version as it took to write it initially. The anticipated speed up is a factor of three for each module.

   i. Can both modules be optimized prior to the one year ship date (two more months)? [7]
   ii. What is the anticipated execution time after the tuning has been performed? (even if it is past the deadline) [6]

b) Syntax and Semantic error messages refer to source code line numbers. Illustrate how these numbers affected by Macro Expansion? [4]

c) Distinguish between the relocation and external reference problem with respect to linker functions [4]

d) Describe static binding giving an advantage and a disadvantage. [4]

Question 5

a) Using Amdahl's law on a given program which has 400 lines of sequential code and 400 lines of parallel:

   i. What is the speed up anticipated with two processors? [5]
   ii. What about 4 processors? [4]
   iii. How many processors would result in a 4-fold speedup? [4]

b) Eight (8) CPUs are connected by a bus whose bandwidth is *r* MB/sec, by what percentage has the bandwidth changed if the system is scaled to 34 CPUs. [6]

c) Describe with illustration a snooping cache and the *write through* protocol? [6]

END OF EXAM ---------- ---------- TOTAL: 100 MARKS