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UNIVERSITY OF SWAZILAND

Faculty of Science
Department of Computer Science

Supplementary Examination, July 2011

Title of paper: **COMPUTER ORGANISATION I**

Course numbers: **CS241**

Time allowed: 3 hours

Instructions: Answer any 4 out of the 5 questions. Each question carries 25 marks.

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Question 1

a) Define the following terms:
   i. Integrated circuit

   ii. LSI

   iii. Programmable Logic Array

   iv. Comparator

   v. Asymmetric clock [5]

b) Draw a diagram showing a NAND gate constructed using 2 transistors. [4]

c) Draw a circuit diagram of an 3-to-8 decoder. [8]

d) Draw a circuit diagram of a 1-bit left/right shifter. It must input a 4-bit value. [8]

Question 2

a) Suppose that the following byte values (shown in hexadecimal) are found in 4 consecutive memory locations starting at address 512:

10 20 04 08

i. What is the 2-byte value at address 514, assuming little-endian representation?

ii. What is the 4-byte value at address 512, assuming big-endian representation? [2]

b) Discuss the 3 main factors that are seen to vary across the memory hierarchy. [6]

c) Distinguish between each of the following pairs:

i. Bus master and slave.

ii. Synchronous and asynchronous buses. [4]

d)

i. What is bus arbitration, and why it is needed? [2]

ii. With the aid of a diagram, describe how bus arbitration can be carried out by daisy chaining. [5]

e) Define each of the following, and explain how each one can improve the performance of computers:

i. Cache

ii. Multiprocessing [6]

Question 3

a) State the full name and purpose of the following pins in memory chips: OE, RAS and CAS. [3]

b) Give 2 reasons why DRAM is preferable to SRAM in cell phones. [2]

c) List any 4 kinds of ROM chips, and describe the main characteristic of each. [8]

d) An FPM-type memory chip has 4 pins for address input and 8 pins for data input/output.

i. Draw the pin diagram of the chip including strobe lines. [3]

ii. Work out the memory capacity of this chip. [2]

e) Draw a diagram of a 2-bit register chip comprised of D flip-flops. It should have a total of 8 pins numbered as follows:

- pins 1 and 2 for data input
- pin 3 for clock (writing to register is enabled at high-to-low transition)
- pin 4 for ground
- pins 5 and 6 for data output
- pin 7 for clear (forces 00 data to be written into register)
- pin 8 for power

Clearly show connections from pins to flip-flops (except power and ground). [7]

Question 4

a) What is the main difference between the B and C buses of the Mic-1 CPU? [1]

b)

i. What roles do the two Mic-1 registers, MPC and MIR, play in controlling the execution of microprograms? [2]

ii. MIR is divided into 6 fields. What is the purpose of each field? [6]

iii. Draw the timing diagram of a single data path cycle in Mic-1. On the diagram, indicate the timing of the following events:
- Updating MPC.
- Updating MIR.
- Propagating control signals. [3]

c)

i. Discuss the role played by the following Mic-1 registers in accessing main memory: MAR, MDR, PC and MBR. [4]

ii. Explain the reason for the following observation: 'When the Mic-1 initiates a memory read operation in cycle *k*, the result only becomes available for use in cycle *k*+2.' [2]

d) What work is done by a microcode assembler? [1]

e) The following Mic-1 microinstruction will lead to the propagation of several control signals. For each control signal, precisely state where it will be directed, and what effects it will cause upon arrival.

MDR = OPC = H + TOS; wr [6]

Question 5

Write four Mic-1 microprograms to carry out the following tasks:

a) Swap the OPC and CPP registers. [3]

b) Compute -(H+TOS-MDR) and write the result to H. [4]

c) Swap the contents of addresses 0 and 1 in main memory. [8]

d) Check whether H register is zero. If so, write 1 to H, otherwise multiply H by 2. [10]

***** END OF PAPER *****

Mic-1 Data Sheet – List of ALU Functions

A, B, $\bar{A}$, $\bar{B}$,
$A+B$, $A+B+1$, $A+1$, $B+1$,
$B-A$, $B-1$, $-A$,
A AND B, A OR B,
0, 1, -1

(The ALU's left and right inputs are denoted A and B, respectively.)
